from passing to the amplifier. In the GND position, S5 opens the signal path and connects the input of the amplifier to ground. This provides a ground reference without the need to disconnect the applied signal from the input connector. Resistor R4, connected across the input coupling switch, allows C3 to be pre-charged in the ground position so that the trace remains on screen when switched to the AC position.

Input Attenuator

The effective overall deflection factor of each channel of the 465 is determined by the appropriate VOLT/DIV switch. The basic deflection factor of the Vertical Deflection System is 5 mV/division of CRT deflection. To achieve the deflection factor values indicated on the front panel, precision attenuators are switched in to the circuit and the gain of the First Cascode Amplifier stage is changed.

For the VOLT/DIV switch positions above 5 mV, attenuators are switched in to the circuit, singly or in pairs, to help produce the vertical deflection factors indicated on the front panel. These attenuators are frequency-compensated voltage dividers. In addition to providing constant attenuation at all frequencies within the bandwidth of the instrument, the Input Attenuators are designed to maintain the same input RC characteristics (1 MΩ times approximately 20 pF) for each setting of the VOLT/DIV switch. Each attenuator contains an adjustable series capacitor to provide correct attenuation at high frequencies and an adjustable shunt capacitor to provide correct input capacitance.

NOTE

Each attenuator is a hybrid encapsulated plug-in assembly; therefore, replacement of individual components within the attenuator is not possible. Should defects occur, the attenuator must be replaced as a unit.

Scale-Factor Switching Circuit

The vertical deflection factor for each channel is indicated by back-lighting the appropriate figures imprinted on the flange of the VOLTS/DIV knob. When a X1 probe is connected to the CH 1 OR X input connector, the base level of transistor Q386 is determined by the voltage divider composed of R384, R383 and X10 display factor bulb DS382. Q386 is biased into saturation and conducts current through the X1 indicator DS386. When Q386 conducts, the voltage level at its collector is very close to +5 volts. Therefore, there is insufficient bias at the base of Q382 to cause Q382 to conduct, and the X10 indicator DS382 remains dark.

When a X10 probe with a scale factor switching connector is attached to the CH 1 OR X input connector, the base of Q382 is returned to ground through R381. Q382 is now biased into saturation and conducts current through X10 indicator DS382. The collector level of Q382 is very close to +5 volts; therefore, there is insufficient bias at the base of Q386 to cause it to conduct and X1 indicator DS386 remains dark.

Source Follower Stage

The Channel 1 signal from the Input Attenuator is connected to the Source Follower Stage through R16 and C16. R15 provides the input resistance for this stage. R16 limits the current drive to the gate of Q20A. Diode CR18 protects the circuit by clamping the gate of Q20A at about −8.7 volts if a high amplitude negative-going signal is applied to the CH 1 OR X input connector. Q20B is a relatively constant current source for Q20A.

First Cascode Amplifier Stage

The Paraphase Amplifier Stage composed of Q32 and Q36 converts the single-ended input signal into a push-pull output signal. C33, C34 and CR34 optimize high frequency response through the amplifier stage. R37 and R38 provide thermal balance for the amplifier. C37 and C38 minimize Miller effect through Q32 and Q36. Step Atten Bal adjustment R25 adjusts for no baseline shift of a CRT display when switching between adjacent positions of the VOLTS/DIV switch.

The Common Base Amplifier stage composed of Q42 & Q44 converts the input signal currents into output voltage signals across load resistors R44 and R45. Correct vertical deflection factors are obtained by using a combination of attenuation in the Input Attenuator Stage and changing the gain of the first Cascode Amplifier Stage. For example, when switching from 50 mV/division to 100 mV/division, the input attenuator remains the same but R46 is switched in parallel with R44 and R45. This divides the output load resistance of the Common Base Amplifier Stage by two, thereby reducing the gain of the stage by two. C46, C47, C48, C49, R47 and R48 provide optimum high frequency response through the channel amplifier when operating with reduced gain.

Second Cascode Amplifier

Transistors Q102-Q122 and Q104-Q124 constitute the Second Cascode Amplifier stage of the Channel 1 vertical preamplifier. Gain adjust R118 sets the overall gain of the Channel 1 vertical preamplifier by adjusting the signal current into the emitters of Q122 and Q124. The VAR control R112, when rotated out of the calibrated detent

position, also adjusts the signal currents into Q122 and Q124 to provide uncalibrated deflection factors between the calibrated settings of the VOLTS/DIV switch. Variable balance adjustment R120 adjusts for no baseline shift of a CRT display when rotating the VAR control. Position Centering adjustment R115 centers the range of control of the Channel 1 POSITION control.

Third Cascode Amplifier

Q132 and Q134, in conjunction with Q304 and Q308 in the Vertical Switching Circuit, form the Third Cascode Amplifier stage. Thermistor RT131 (between the emitters of Q132 and Q134) changes in value with changes in temperature. This varies the gain of the Third Cascode Amplifier stage to compensate for changes in total amplifier gain that occur with variations in operating temperature. The push-pull signals picked off in the emitters of Q132 and Q134 are converted to a single-ended signal by Q142 and Q148. This signal is amplified by common-base amplifier stage Q152 and applied to the bases of emitter followers Q162 and Q164. Q164 provides the output signal to the CH 1 VERT SIGNAL OUT connector located on the instrument rear panel. The output signal at the emitter of Q162 is used as the trigger signal source in the CH 1 positions of the Trigger SOURCE switches and as the signal source for emitter follower Q168. Q168 provides the X-axis signal from the Channel 1 Preamplifier to the Horizontal Amplifier in the X-Y mode of operation. CR164, CR165, CR166, and CR167 protect the emitter circuit of Q164 in the event large voltage levels are accidentally connected to the CH 1 VERT SIGNAL OUT connector. R155 adjusts the DC level of the CH 1 trigger source signal.

CHANNEL 2 PREAMP

General

The Channel 2 Preamp circuit is basically the same as the Channel 1 Preamp. Only the specific differences between the two circuits are described here. Portions of this circuit not described in the following description operate in the same manner as for the Channel 1 Preamp. Fig. 3-3 shows a detailed block diagram of the Channel 2 Preamp circuit. A schematic of this circuit is shown on diagram 2 at the rear of this manual.

Second Cascode Amplifier

The Second Cascode Amplifier in Channel 2 is basically the same as the Second Cascode Amplifier in Channel 1 except that the Channel 2 INVERT switching takes place here. For a normal (non-inverted) display, +5 volts is connected to the bases of transistors Q222 and Q224 by INVERT switch S225. The voltage divider comprised or R225 and R226 applies approximately +2.5 volts to the base of Q226 and Q228. Q222 and Q224 are biased on and Q226 and Q228 are biased off, and the signal passes on to the output cascode amplifier stage normally. With the INVERT switch in the INVERT (button in) position, +5 volts is applied to the bases of Q226 and Q228. The voltage divider composed of R225 and R224 applies approximately +2.5 volts to the bases of Q222 and Q224. Q226 and Q228 are now biased on and Q222 and Q224 are biased off. The signal that was normally applied to the base of Q232 is now applied to the base of Q234 through transistor Q228 and the signal that was normally applied to the base of Q234 is now applied to the base of Q232 through transistor Q226.

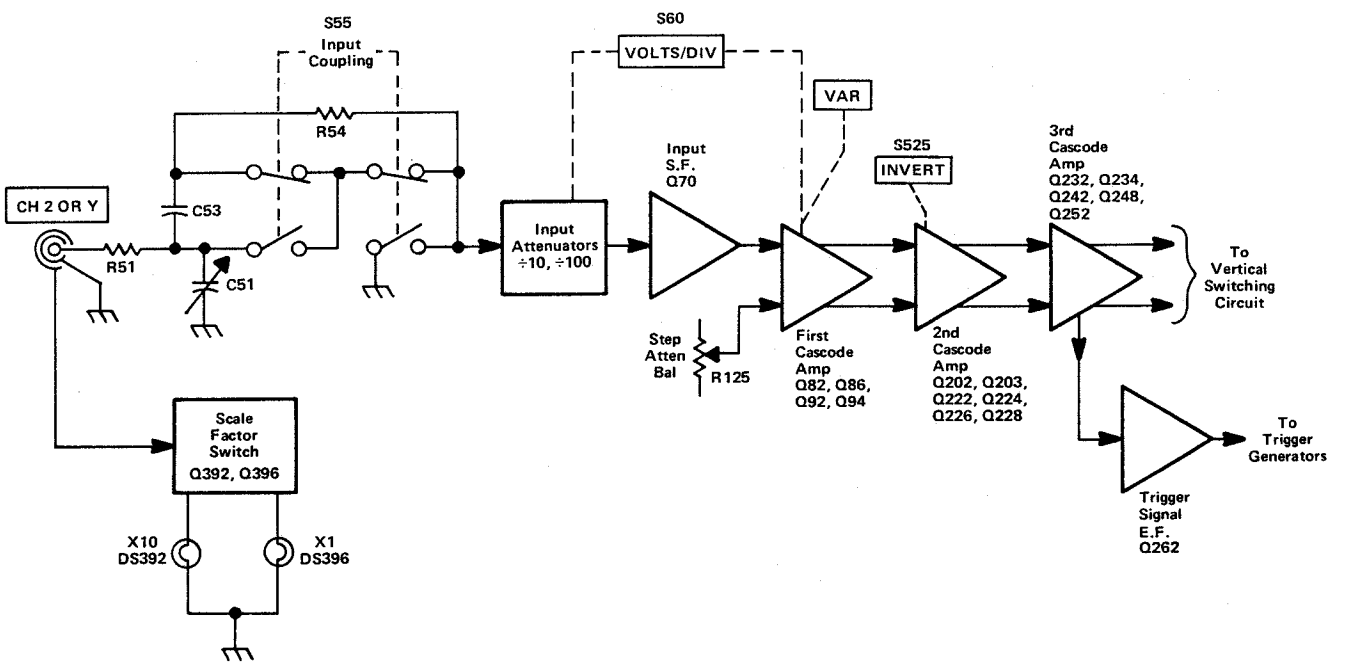

Fig. 3-3. Detailed block diagram of the Channel 2 Preamplifier.

Third Cascode Amplifier

The trigger pickoff circuit only provides a signal to one emitter follower. This emitter follower (Q262) in turn provides the trigger signal to the Trigger Generator circuits in the CH 2 positions of the SOURCE switches.

VERTICAL SWITCHING CIRCUIT

General

The Vertical Switching Circuit determines whether the Channel 1 or Channel 2 or both signals are connected to the Vertical Output Amplifier Circuit. In the alternate and chopped modes of operation both channels are alternately displayed on a shared time basis. Fig. 3-4 shows a detailed block diagram of the Vertical Switching Circuit. A schematic of this circuit is shown on diagram 3 at the rear of this manual.

Diode Gates

The Diode Gates, consisting of four diodes each, can be thought of as switches which allow either of the Vertical Preamp output signals to be coupled to the Vertical Output Amplifier. CR304, CR305, CR307 and CR308 control the Channel 1 output and CR314, CR315, CR317 and CR318 control the Channel 2 output. These diodes are in turn controlled by the Switching Multivibrator for dual trace displays, or by the VERT MODE switch for single trace displays.

Channel 1 Only Display. When the CH 1 pushbutton is pressed, –8 volts is applied to the junction of CR315-CR317 in the Channel 2 Diode Gate through R367 (see simplified diagram in Fig. 3-5). This forward biases CR315 and CR317 and reverse biases CR314 and CR318. CR314 and CR318 block the Channel 2 signal so it cannot pass to the Delay Line Driver stage. At the same time in the Channel 1 Diode Gate, CR305 and CR307 are connected to +5 volts through R371. CR305 and CR307 are held reverse-biased while CR304 and CR308 are forward biased. Therefore, the Channel 1 signal passes to the Delay Line Driver stage.

Channel 2 Display Only. When the CH 2 pushbutton is pressed, the above conditions are reversed. The junction of CR305-CR307 is connected to –8 volts through R376 and

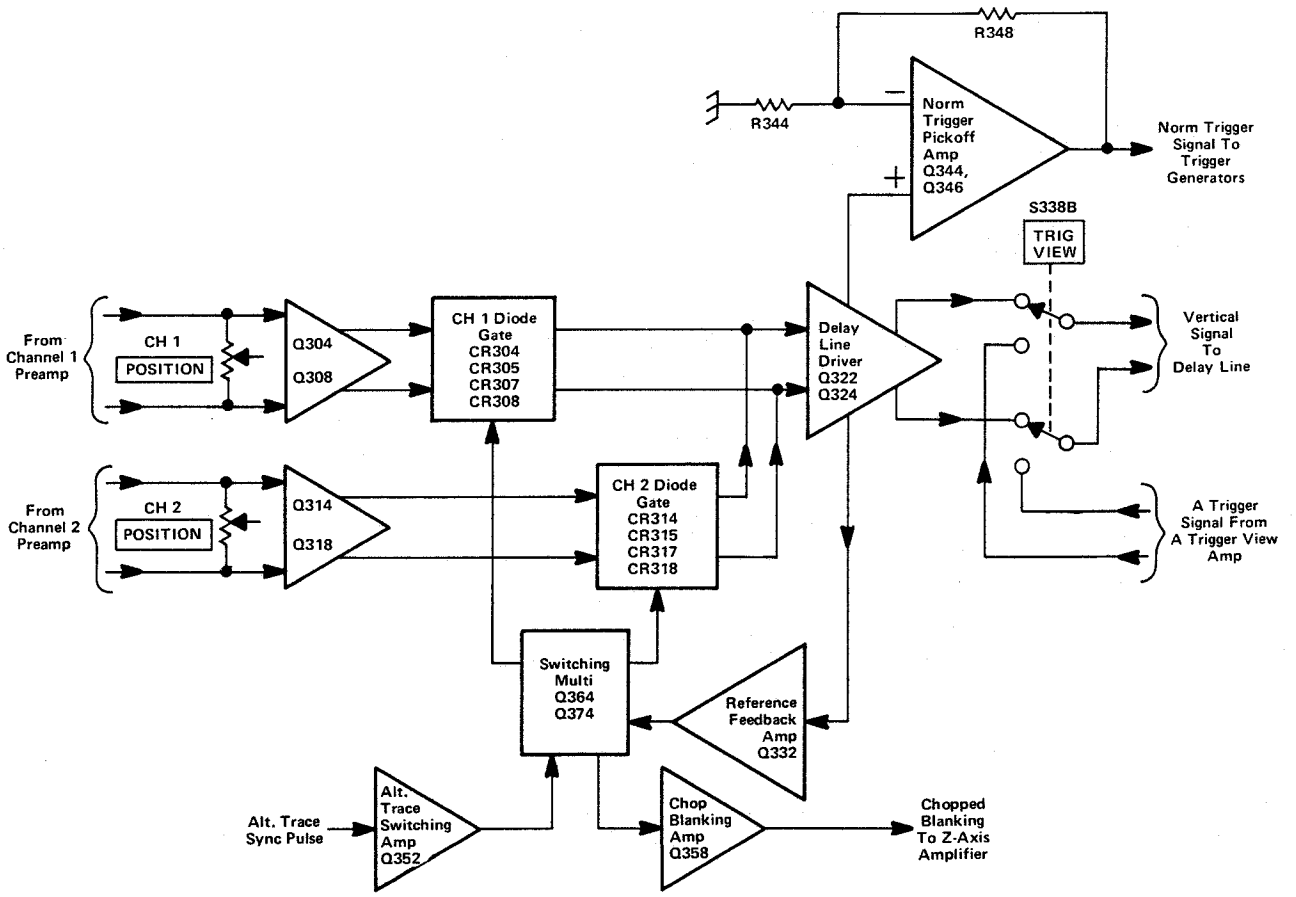

Fig. 3-4. Detailed block diagram of the Vertical Switching Circuit.

the junction of CR315-CR317 is connected to +5 volts through R361. The Channel 1 Diode Gate blocks the Channel 1 signal and the Channel 2 Diode Gate allows the Channel 2 signal to pass to the Delay Line Driver stage.

Switching Multivibrator

Alternate Trace Display. In this mode of operation, the Switching Multivibrator operates as a bistable multivibrator. When the ALT pushbutton is pressed, –8 volts is applied to the emitter of Alternate Trace Switching Amplifier stage Q352 by the VERT MODE switch. Q352 is forward biased to supply current to the "on" Switching-Multivibrator transistor through R352 and CR368 or CR378. For example, if Q374 is conducting, current is supplied to Q374 through R352 and CR378. The current flow through collector resistor R371 drops the CR305-CR307 cathode level negative so that the Channel 1 Diode Gate is blocked as for Channel 2 Only Operation. The signal passes through the Channel 2 Diode Gate to the Delay-Line Driver stage.

The alternate trace sync pulse is applied to the base of Q352 through C351 at the end of each sweep. This negative-going sync pulse momentarily interrupts the current through Q352 and both Q364 and Q374 are turned off. When Q352 turns on again after the alternate trace sync pulse, the charge on C368 determines whether Q364 or Q374 conducts. For example, when Q374 was conducting, C368 was charged positive on the CR378 side to the emitter level of Q374 and negatively on the CR368 side toward the negative level at the junction of CR368 and CR378. This charge is stored while Q352 is off and holds the emitter of Q364 more negative than the emitter of Q374. During the time Q364 and Q374 are turned off, the voltages at their bases become approximately equal. Now, when Q352 comes back on, the transistor with the most negative emitter conducts first, the resulting negative movement at its collector holds the other transistor off. The conditions described previously are now reversed: now, the Channel 2 Diode Gate is reverse-biased and the Channel 1 signal passes through the Channel 1 Diode Gate.

Chopped Mode Operation. When the CHOP pushbutton is pressed, the Switching Multivibrator stage free-runs at about a 250 kHz rate. The emitters of Q364 and Q374 are connected to –8 volts through R368, R378, and the primary of transformer T354. At the time of turn-on, one

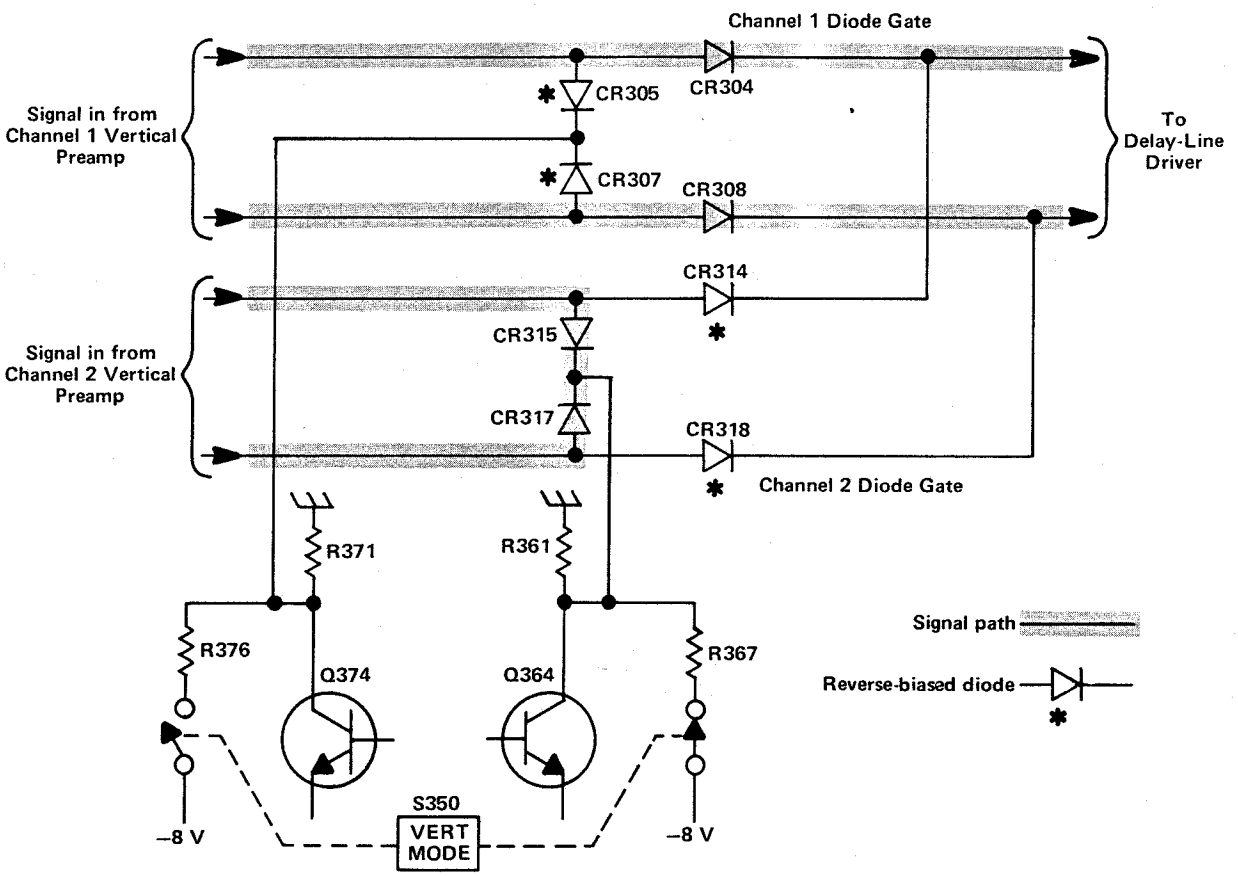

Fig. 3-5. Effect of Diode Gates on signal path (simplified Vertical Switching diagram). Conditions shown for CH 1 position of VERT MODE switch.

of the transistors begins to conduct; for example, Q374. The negative level at the collector of Q374 forward-biases CR305 and CR307 and back-biases CR304 and CR308 preventing the Channel 1 signal from reaching the Delay-Line Driver stage. Meanwhile, the Channel 2 Diode Gate passes the Channel 2 signal to the Delay-Line Driver stage.

The frequency-determining components in the CHOP mode are C368, R368, R370, and R378. The switching action occurs as follows: when Q374 is on, C368 attempts to charge to −8 volts through R368. The emitter of Q364 slowly goes toward −8 volts as C368 charges. The base of Q364 is held at a point determined by the voltage divider R365 and R374 between −8 volts and the collector level of Q374. When the emitter voltage of Q364 reaches a level slightly more negative than its base, Q364 conducts. Its collector level goes negative and pulls the base of Q374 negative through divider R364-R375 to cut Q374 off. This switches the Diode Gate stages to connect the opposite channel to the Delay-Line Driver stage. Again, C368 begins to charge towards −8 volts but this time through R378. The emitter of Q374 slowly goes negative as C368 charges until Q374 turns on. Q364 is shut off and the cycle begins again.

The Chop Blanking Amplifier stage, Q358, provides an output pulse to the Z Axis Amplifier circuit which blanks out the transition between the Channel 1 and the Channel 2 traces. When the Switching Multivibrator stage changes states, the voltage across T354 momentarily increases. A negative pulse is applied to the base of Q358 to turn it off. The width of the pulse at the base of Q358 is determined by R356 and C356. Q358 is quickly driven in to cutoff and the positive going output pulse, which is coincident with trace switching, is connected to the Z Axis Amplifier circuit through R359.

Added Mode Operation. When the ADD pushbutton is pressed, the following occurs:

1. +5 volts is applied to the cathodes of CR305 and CR307 through R371.

2. +5 volts is applied to the cathodes of CR315 and CR317 through R361.

3. −8 volts is applied to the junction of R321 and R322.

The first two actions enable both of the Channel Diode Gates so that the signal applied to the Delay Line Driver stage is the algebraic sum of the Channel 1 and Channel 2 signals. The −8 volts applied to R321 and R322 provides sufficient current to keep both diode gates turned on without altering the DC levels associated with the Delay Line Driver stage.

Delay-Line Driver

The outputs from the Diode Gate stages are applied to the Delay-Line Driver stage composed of Q322 and Q324. Q322 and Q324 are connected as feedback amplifiers with R325 and R327 providing feedback from the collector to the base of their respective transistors. A sample of the signal in the collector circuit of Q322 is used for triggering in the NORM mode of trigger operation. The BW LIMIT switch S338A connects a pi filter composed of C338, C339, L338, and L339 between the output signal lines of the Delay-Line Driver stage to reduce the upper −3 dB bandwidth limit of the Vertical Amplifier system to approximately 20 MHz. R335 and R336 provide reverse termination for the delay line. The TRIG VIEW switch S338B connects the output of the Trigger View Amplifier to the input of the Delay Line in place of the Delay Driver Stage. This allows viewing the trigger signal present in the A Trigger Generator Circuit.

Reference Feedback Amplifier

Reference Feedback stage Q332 provides common mode voltage feedback from the Delay-Line Driver stage to allow the diode gates to be switched with a minimum amplitude switching signal. The emitter level of Q332 is connected to the junction of the Switching Multivibrator collector resistors, R371 and R361 through CR372 or CR362. The collector level of the "on" Switching Multivibrator transistor is negative and either CR362 or CR372 is forward biased. This clamps the cathode level of the forward biased shunt diodes in the applicable Diode Gate about 0.5 volt more negative than the emitter level of Q332. The level at the emitter of Q332 follows the average voltage level at the emitters of the Delay-Line Driver stage. The shunt diodes are clamped near their switching level and therefore, can be switched very fast with a minimum amplitude switching signal. This maintains about the same current through the Diode Gate shunt diodes so they can be switched with a minimum amplitude switching signal regardless of the deflection signal at the anodes of the shunt diodes.

Normal Trigger Pickoff Amplifier

The trigger signal for NORM trigger operation is obtained from the collector of Q322. Normal Trigger DC Adjustment R340 sets the DC level of the normal trigger output signal so the sweep is triggered at the 0 level of the displayed signal when the Triggering LEVEL control is set to 0. Q344 and Q346 are connected as a feedback amplifier with the signal applied to the non-inverting input and the feedback connected between the output and the inverting input. Gain of the stage is approximately:

$$\frac{R348 + R344}{R344}$$

VERTICAL OUTPUT AMPLIFIER

General

The Vertical Output Amplifier circuit provides the final amplification for the vertical deflection signal. This circuit includes the Delay Line and the BEAM FIND pushbutton. The BEAM FIND pushbutton compresses an overscan

display to within the viewing area when pressed. A schematic of the Vertical Output Amplifier circuit is shown on diagram 4 at the rear of this manual.

Delay Line

Delay Line DL400 provides approximately 120 ns delay for the vertical signal to allow the Sweep Generator circuits time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the CRT. This allows the instrument to display the leading edge of the signal originating the trigger pulse when using internal triggering.

Output Amplifier

U440 is an integrated circuit amplifier stage that provides the final amplification for the vertical signal. R401 and R411 provide forward termination for the delay line. The components connected between pins 2 and 4 of U440 provide delay-line compensation. Components connected between pins 14 and 15 and pins 7 and 8 of U440 provide thermal compensation for the stage. The BEAM FIND switch, when pressed, reduces the dynamic swing capabilities of the stage, thereby limiting the display to within the display area of the CRT.

A AND B TRIGGER GENERATORS

General

The Trigger Generator circuits produce trigger pulses to start the Sweep Generator circuits. These trigger pulses are derived either from the internal trigger signal from the vertical deflection system, an external signal connected to the external trigger input connectors, or a sample of the line voltage applied to the instrument. Controls are provided in each circuit to select trigger level, slope, coupling, and source. Since the A and B Trigger Generator circuits are virtually the same, only the A Trigger Generator circuit action and the differences between the A and B Trigger Generator circuits are explained. A schematic of these circuits is shown on diagram 5 at the back of this manual.

Trigger Source

The Trigger SOURCE switch S610 selects the source of the trigger signal. The sources available to the A Trigger Generator circuit are the signal(s) being displayed (NORM), Channel 1 (CH 1), Channel 2 (CH 2), LINE, and EXT. The EXT ÷ 10 (A trigger circuit only) position provides 10 times attenuation for the external trigger signal. The B Trigger SOURCE switch does not have a LINE or an EXT ÷ 10 position, but has a STARTS AFTER DELAY position.

In the LINE mode of triggering, a sample of the power line frequency is obtained from the secondary of power transformer T1501 in the Low Voltage Power Supply circuit. To prevent unwanted attenuation of the trigger signal by the LF REJ circuit, the Trigger COUPLING switches should not be in the LF REJ mode when using line voltage as a trigger source.

Trigger Coupling

The Trigger COUPLING switches offer a means of accepting or rejecting certain components of the trigger signal. In the AC, LF REJ, and HF REJ mode of trigger coupling, the DC component of the trigger signal is blocked by coupling capacitors C612 or C611. Frequency components below about 60 Hz are attenuated when using AC or HF REJ coupling and below about 15 kHz when using LF REJ coupling. The higher frequency components of the trigger signal are passed without attenuation. In the HF REJ mode of trigger coupling, the high frequency components of the trigger signal (above about 50 kHz) are attenuated, while the lower frequency components are passed without attenuation. The DC mode of trigger coupling passes unattenuated all signals from DC to 100 MHz and above.

Input Source Follower

Transistor Q622 is an FET source follower. It provides a high input impedance (set primarily by R616) for the trigger signal and also provides isolation between the Trigger Generator circuit and the trigger signal source. Diode CR617 provides input protection for Q622 if excessively high amplitude negative-going input signals are present. Q624 is a high-impedance, relatively constant, current source for Q622, and provides a measure of temperature compensation for Q622.

Paraphase Amplifier

U640 is a paraphase amplifier stage that converts the single-ended input from Source Follower Q622 into a push-pull output applied to the tunnel diode driver stage. Trigger Level Centering adjustment R635 sets the level at pins 14 and 15 of U640 so that the display is correctly triggered when the LEVEL control is centered. The LEVEL control varies the level at pins 14 and 15 of U640 to select the point on a trigger signal where triggering occurs.

The slope of the input signal that triggers the Sweep Generator circuit is determined by the setting of the SLOPE switch S630. When the SLOPE switch is set to the + position, the output signal present at pin 8 of U640 is in phase with the input signal and the output signal at pin 9 is

inverted with respect to the input signal. When the SLOPE switch is set to the – position, the output signal at pin 8 is inverted with respect to the input signal and the output signal at pin 9 is in phase with the input signal.

Tunnel Diode Driver

Q650 and Q652 are common-emitter amplifier stages that provide the signal currents necessary to switch the triggering tunnel diodes. CR650 and CR652 are 4.7 mA tunnel diodes. Quiescently (i.e., after the sweep holdoff period has passed, but before triggering), CR650 and CR652 are biased into their low voltage states. Q650 cannot provide sufficient current to switch CR650 to its high voltage state. Q652, however, can provide sufficient current to bias CR652 into its high voltage state; when Q652 next conducts triggering signal current, the anode of CR652 steps positive to an approximate +0.5 volt level. Since only approximately 1 mA of current is required to maintain CR652 in its high voltage state, this makes approximately 3 mA of current additionally available with which to switch CR650 to its high voltage state. Thus, the next time Q650 conducts signal current, CR650 steps to its high voltage state, sending a positive pulse to the logic circuit to initiate sweep action. A Trigger Sensitivity adjustment R655 adjusts the tunnel diode bias to the proper level that will not allow CR650 to be switched to its high voltage state until CR652 has been switched to its high voltage state. At the end of the sweep time and during holdoff, a negative level is applied to the anode of CR652, thereby resetting both CR650 and CR652 to their low voltage states. The reset level remains during holdoff time to ensure that a sweep gating signal will not be generated until the sweep circuit has returned to its quiescent state.

A AND B SWEEP GENERATORS

General

The A and B Sweep Generators produce sawtooth voltages which are amplified by the Horizontal Amplifier circuit to provide horizontal deflection on the CRT. These sawtooth voltages are produced on command (trigger pulses) from the Trigger Generator circuits. The Sweep Generator circuits also produce gate waveforms that are used by the Z Axis Logic circuit to unblank the CRT during sweep time, and by the Sweep Logic circuit to terminate sweep generation. Fig. 3-6 shows a detailed block diagram of the A Sweep Generator circuit. The B Sweep Generator circuit is very similar to the A Sweep Generator; therefore only the differences in operation associated with the B Sweep Generator will be discussed. A schematic of both circuits is shown on diagram 6 at the rear of this manual.

Disconnect Amplifier

After holdoff but before the next sweep, Disconnect Amplifier Q1024 conducts current through R1024 and the timing resistor R_t. This prevents timing current from

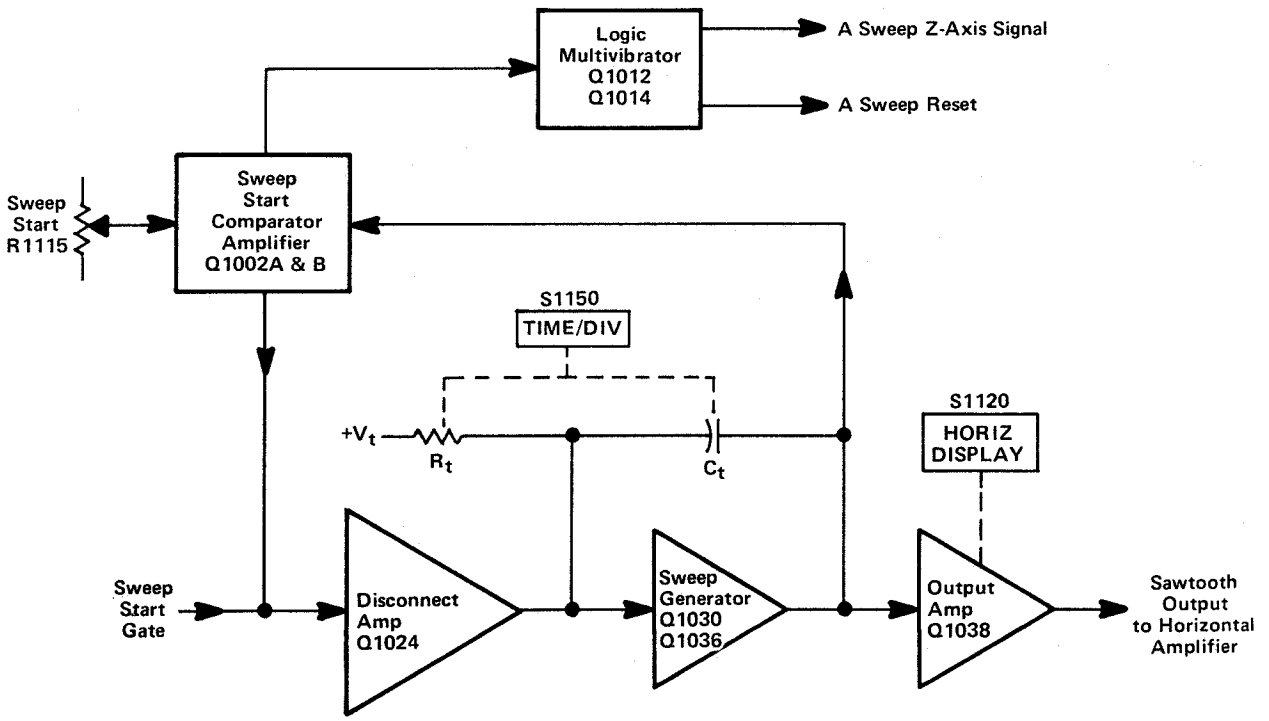

Fig. 3-6. Detailed block diagram of the A Sweep Generator.

charging the timing capacitance C_t. The positive-going sweep start gate from Q864 turns off Q1024 and the timing current now begins to charge the timing capacitance.

Sawtooth Sweep Generator

Q1030 and Q1036 compose a Miller Integrator circuit. When the current flow through the Disconnect Amplifier is interrupted, the timing capacitance begins to charge through the timing resistor. The timing resistor and capacitance are selected by the A TIME/DIV switch to provide the various sweep rates listed on the instrument front panel. The output signal at the collector of Q1036 is a negative-going sawtooth waveform.

Output Buffer Amplifier

The Output Buffer Amplifier stage is a common-base amplifier with the signal current-driven into the emitter. It provides the output sawtooth current signal to the Horizontal Amplifier and provides a measure of isolation between the Sawtooth Generator and the Horizontal Amplifier. The HORIZ DISPLAY switch connects to this stage to control the A sawtooth output in the various horizontal modes of operation. In the A and A INTEN modes of operation, the A sweep signal passes through Q1038 to the Horizontal Amplifier. However, in the MIX and B DLY'D modes, –8 volts is connected to zener diode VR1039 which sets the emitter of Q1038 at about –1.8 volts. This biases Q1038 off, preventing the A sawtooth signal from passing to the Horizontal Amplifier.

Sweep Start Amplifier

Just before the sweep starts to run down, the levels at the bases of Q1002 A and B are approximately equal. When the sweep starts to run down, the base of Q1002B goes negative, which increases the forward bias on CR1004. This in turn decreases the forward bias on CR1001, which, very shortly after the start of the sweep, becomes reverse biased to interrupt the current through Q1002A. The circuit remains in this condition until after the sweep retrace is complete. When the circuit returns to quiescence, Q1002A again begins to conduct through R1024. This sets the current through Q1024, which establishes the starting point for the sweep. The Sweep Start adjustment sets the base level of Q1002A. This level is also connected to the base of Q1062A in the B Sweep Generator except in the MIX mode of operation. This ensures that B Sweep starts at the same level as A Sweep.

Logic Multivibrator

Q1012 and Q1014 compose a multivibrator. At quiescence, Q1014 is conducting and Q1012 is turned off. When the sweep starts to run, the negative-going ramp is coupled through the base of Q1002B and CR1004 to the cathode of CR1011. CR1011 becomes forward biased and when the level at the anode of CR1011 falls to about +4 volts Q1012 conducts and Q1014 turns off. The multivibrator remains in this state until the sweep starts to retrace and the voltage level at the anode of CR1011 rises above about +4.5 volts. The resultant pulse at the collector of Q1012 is applied to Sweep Control IC U870 to terminate the sweep. The pulse at the collector of Q1014 is applied to the A Sweep Z Axis Logic Gate to blank the CRT at the end of the sweep.

B Sweep Generator Differences

There are three prime differences between the A and B Sweep Generators. The B Sweep Output Buffer Amplifier is prevented from passing the B Sweep signal to the Horizontal Amplifier in the A and A INTEN positions of the HORIZ DISPLAY switch. There is a transistor stage connected as a constant current source in the emitter circuit of Q1062A and B (corrects for current imbalances side-to-side in Q1062 during MIX mode operation). The Sweep Start Level connected to the base of Q1062A is not always a fixed DC level. During MIX mode operation the A Sweep Sawtooth signal is applied to the base of the amplifier. Now, the DC level at which the B Sweep Generator will start generating its sawtooth waveform is constantly being changed by the A Sweep sawtooth. The output waveform from the B Sweep Generator takes the form of a composite sawtooth waveform, with the first and last parts occurring at a rate determined by the A Sweep Generator and the middle part occurring at a rate determined by the B Sweep Generator.

SWEEP AND Z AXIS LOGIC CIRCUIT

General

The Sweep And Z Axis Logic Circuit derives the logic levels necessary to control the sequence of events associated with sweep generation and CRT unblanking. The +A and +B GATE signals are also generated in this circuit. Positive logic terminologies and symbologies will be used in the following explanation of circuit operation. A schematic of this circuit is shown on diagram 8 at the rear of this manual.

A Sweep Gate

Q862 and Q864 compose the A Sweep Gate Circuit. They form an emitter coupled stage where only one transistor can be conducting at any time. The input signal to the stage is the positive-going trigger signal from the A Fire Trigger TD in the A Trigger Generator Circuit. The

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signal at the collector of Q862 is connected to the A Z Axis Gate Circuit to control CRT blanking and to generate the + A GATE signal. The signal at the collector of Q864 is connected to the emitter of the Sweep Disconnect Amplifier stage (Q1024) in the A Sweep Generator Circuit to initiate A Sweep generation.

B Sweep Gate

Q812 and Q814 compose the B Sweep Gate Circuit. They also form an emitter-coupled stage where only one transistor can be conducting at any time. The input signal to the stage is the positive-going trigger signal from the B Fire Trigger TD in the B Trigger Generator Circuit. The signal at the collector of Q812 is connected to the B Z Axis Gate Circuit to control CRT blanking and to generate the + B GATE signal. The signal at the collector of Q814 is connected to the emitter of the Sweep Disconnect Amplifier stage (Q1084) in the B Sweep Generator Circuit to initiate B Sweep generation.

Sweep Control Integrated Circuit

U870 is the Sweep Control Integrated Circuit. Several functions are performed in this stage, depending on the mode of operation of the instrument sweep generators. The following is a brief explanation of the function associated with each pin of the IC.

Pin 1. This is the positive Auto Sense input. The signal connected here comes from the A Fire Trigger TD.

Pin 2. This is the negative Auto Sense input. A fixed DC level established by R871 and R872 is connected here.

Pin 3. This is the + auto gate terminal. In the AUTO mode of operation, if no trigger signals are applied to pin 1 of U870 during the ≈100 ms following the end of holdoff the gate level at pin 3 steps LO to turn Q864 on which initiates a sweep.

Pin 4. Not used in this application.

Pin 5. Input terminal for negative voltage supply.

Pin 6. This is the auto gate timing terminal. R879 and C879 determine the amount of time between the end of holdoff and the generation of the auto gate.

Pin 7. This terminal lights the TRIG'D light when a triggered gate has occurred.

Pin 8. This is the holdoff timing terminal. The R/C connected to this terminal (selected by the TIME/DIV switch) determines the length of holdoff time.

Pin 9. Ground terminal.

Pin 10. This is the Holdoff output terminal. The gate level present here is LO during sweep holdoff time and HI otherwise.

Pin 11. This terminal lights the READY light when operating in the single sweep mode.

Pin 12. This is the single sweep mode terminal. When +5 volts is applied to this terminal the sweep operates in the single sweep mode; when the terminal is left open or grounded the sweep operates in the repetitive mode.

Pin 13. Not used in this application.

Pins 14 & 15. Single sweep reset terminals. Pushing the PUSH TO RESET button prepares the single sweep circuitry to respond to the next one triggering event. Also causes the READY light to be lit.

Pin 16. This is the holdoff start input terminal. The HI sweep reset gate pulse from the sweep generators is applied here to initiate sweep holdoff.

Pin 17. This is the sweep disable output terminal. The gate level at this terminal is HI during holdoff and LO otherwise.

Pin 18. Sweep lockout input. +5 volts applied to this terminal disables all sweep action.

Pin 19. Auto mode terminal. Grounding this terminal enables auto sweep operation.

Pin 20. Input terminal for positive voltage supply.

A Sweep Holdoff Amplifier

Q854 is the A Sweep Holdoff Amplifier. The holdoff gate waveform is applied to the base of Q854 through R858 and C858 from pin 17 of U870. When Q854 is turned off (during holdoff time), its collector is LO and CR851 is forward biased, which resets both the Arm and Fire trigger TD's in the A Trigger Generator. When Q854 is turned on (any time other than holdoff time), its collector level is HI and CR851 is reversed biased. This allows the trigger TD's in the A Trigger Generator to respond to the next adequate triggering signal.

B Sweep Holdoff Amplifier

Q804 is the B Sweep Holdoff Amplifier. Its circuit action is identical to that described for the A Sweep Holdoff Amplifier except that there are three gate signal sources that control the state of the stage. The three sources are the holdoff gate from pin 17 of U870 (through CR859), the collector of Q1052 in the Delay Pickoff Comparator, and the collector of Q822 in the B Latch Multivibrator (through CR809). All three gate sources must be in their LO state for B Sweep to be triggerable; any one of the sources in its HI state will disable the B Trigger Generator TD's.

A Sweep Z-Axis Gate

Q1304 and Q1306 comprise the A Sweep Z-Axis Gate. They form an emitter-coupled stage where only one transistor can be conducting at any time. The controlling signal inputs come from the collector of Q862 in the A Sweep Gate, the blanking signal from Q1014 in the A Sweep Generator, and Q824 in the B Latch Multivibrator (only in the MIX mode of operation). The blanking signal for use in the Z-Axis Amplifier is taken from the collector of Q1306 (through CR1342). The collector signal of Q1304 is applied to the +A GATE Emitter Follower.

In all positions of the HORIZ DISPLAY switch except for B DLY'D, –8 volts is connected to the cathode of CR1341. This pulls the anode of CR1306 down very close to –8 volts, causing CR1306 to be reverse biased, which in turn allows the gate signal at the collector of Q1306 to pass through CR1342. In the B DLY'D position of the HORIZ DISPLAY switch, –8 volts is no longer connected to CR1341. This allows CR1306 to be forward biased, which pulls up on the cathode of CR1342. This reverse-biases CR1342, which blocks the A blanking signal from reaching the Z-Axis Amplifier.

In all positions of the HORIZ DISPLAY switch except MIX, –8 volts is connected to the cathode of CR832. This keeps CR831 reverse biased and prevents the collector signal of Q824 from affecting the A Z-Axis Gate. However, in the MIX position of the HORIZ DISPLAY switch, –8 volts is no longer connected to CR832. Now, when the B Sweep ends and sets the B Sweep Latch circuit, the collector signal of Q824 (through CR831) switches the A Sweep Z-Axis Gate causing the CRT display to be completely blanked. This prevents any further display of A Sweep in the MIX mode even though A Sweep may still be running.

B Sweep Z-Axis Gate

Q1324 and Q1326 compose the B Sweep Z-Axis Gate. They form an emitter-coupled stage where normally one transistor is on and the other is off. The controlling signal inputs come from the collector of Q812 in the B Sweep Gate and the blanking signal from Q1074 in the B Sweep Generator. The blanking signal for use in the Z-Axis Amplifier is taken from the collector of Q1326 (through CR1344). The collector signal of Q1324 is applied to the +B GATE Emitter Follower.

In the A position of the HORIZ DISPLAY switch, –8 volts is applied to the cathode of CR1347, which causes CR1345 to be back biased. The collector of Q1326 is pulled positive through R1326 and CR1326, which in turn back biases CR1344, preventing the B Sweep Z-Axis Gate from affecting CRT unblanking. In the MIX and A INTEN positions of the HORIZ DISPLAY switch, –8 volts is removed from the cathode of CR1347 and applied to the cathode of CR1327. This forward biases CR1345 and reverse biases CR1326. CR1344 is still reverse biased, but when B Sweep starts, the collector of Q1326 steps negative enough to forward bias CR1344 and add a slight amount of unblanking to the A Sweep unblanking already present. This provides a measure of intensification for the B Sweep portion of an A INTEN or MIX display. In the B DLY'D position of the HORIZ DISPLAY switch, –8 volts is applied to the cathodes of CR1327 and CR1347. This reverse biases both CR1345 and CR1326, which allows the full B Sweep unblanking signal to pass through CR1344. Since the A Sweep Z-Axis Gate output diode CR1342 is held reverse biased, the only unblanking signal present at the input to the Z-Axis Amplifier will be the B Sweep signal.

+A GATE And +B GATE Emitter Followers

Q1314 and Q1334 are emitter followers providing the +A GATE and +B GATE output signals available at the instrument rear panel. The output signals are positive-going rectangular waveforms, approximately 5.5 volts in amplitude. The amplitude is set in the collectors of Q1304 and Q1324. For example, when Q1304 is conducting the base of Q1314 can go no more negative than approximately –0.7 volt (limited by CR1304). When Q1304 is not conducting, the base of Q1314 rises to the decoupled +5 volts power supply level through R1304. CR1315, CR1316,